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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SHAJAN MATHEW and LAKSHMI KATA BERA

Appeal 2009-0847
Application 10/763,304
Technology Center 2800

Decided:[1] March 27, 2009

Before ROBERT E. NAPPI, JOHN A. JEFFERY, and ELENI MANTIS MERCADER, *Administrative Patent Judges.*

NAPPI, *Administrative Patent Judge.*

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

This is a decision on appeal under 35 U.S.C. § 6(b) of the rejection of claims 1 through 12, 14 through 28, and 31. Claims 13, 29 and 30 have been canceled.

We affirm.

INVENTION

The invention is directed towards a method for forming a metal oxide silicon field effect transistor (MOSFET) having a self aligned metal silicide region on both source/drain and on top of the metal gate. See page 3 of Appellants' Specification. Claim 1 is reproduced below:

> 1. A method of forming a metal oxide semiconductor field effect transistor (MOSFET)
> device on a semiconductor substrate comprising the steps of:
> forming a gate insulator layer on said semiconductor substrate;
> forming a conductive layer on said gate insulator layer, wherein said conductive layer is formed of a single material;
> without inclusion of any interceding steps immediately forming an amorphous silicon layer, wherein said amorphous silicon layer is formed of a single material, directly on said conductive layer;
> defining a conductive gate structure and an overlying amorphous silicon shape, on said gate insulator layer;
> removing portion of said gate insulator layer not covered by said conductive gate structure;
> forming a first doped region in an area of said semiconductor substrate not covered by said conductive gate structure;
> forming composite insulator spacers on the sides of said conductive gate structure and on the sides of said amorphous silicon-shape
> forming a second doped region in an area of said semiconductor substrate not covered by said conductive gate structure, or by said composite insulator spacers;
> forming a metal layer, wherein said metal layer is formed of a single material;
> performing an anneal procedure to form first metal silicide regions from an overlying first portion of said metal layer and from a

top portion of said second doped region, and to form a second metal silicide region directly on said conductive gate structure from an overlying second portion of said metal layer via total consumption of said amorphous silicon shape, while third portions of said metal layer located on said composite insulator spacers remain unreacted; and

removing unreacted portions of said metal layer located on said composite insulator spacers.

REFERENCES

Chau	US 5,625,217	Apr. 29, 1997
Bai	US 5,818,092	Oct. 6, 1998
Nguyen	US 6,084,279	Jul. 4, 2000
Wieczorek	US 6,274,511 B1	Aug. 14, 2001
Tsai	US 2002/0192932 A1	Dec. 19, 2002
Deshpande	US 6,512,266 B1	Jan. 28, 2003

REJECTIONS AT ISSUE

The Examiner has rejected claims 1 through 6, 9 through 12, and 14 under 35 U.S.C. § 103(a) as being unpatentable over Bai and Deshpande. The Examiner's rejection is on pages 4 through 7 of the Answer.[2]

The Examiner has rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Bai, Deshpande, and Wu. The Examiner's rejection is on page 7 of the Answer.

[2] Throughout the opinion we refer to the Answer mailed April 1, 2008.

The Examiner has rejected claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Bai, Deshpande, Tsai, and Wieczorek. The Examiner's rejection is on pages 7 and 8 of the Answer.

The Examiner has rejected claims 16 through 21 and 24 through 28 under 35 U.S.C. § 103(a) as being unpatentable over Bai, Deshpande, and Wieczorek. The Examiner's rejection is on pages 8 and 9 of the Answer.

The Examiner has rejected claim 23 under 35 U.S.C. § 103(a) as being unpatentable over Bai, Deshpande, Wieczorek, and Wu. The Examiner's rejection is on pages 9 and 10 of the Answer.

The Examiner has rejected claim 31 under 35 U.S.C. § 103(a) as being unpatentable over Bai, Deshpande, Wieczorek, and Tsai. The Examiner's rejection is on pages 10 and 11 of the Answer.

The Examiner has rejected claims 1 through 4, 6, 7, and 9 under 35 U.S.C. § 103(a) as being unpatentable over Chau, and Nguyen. The Examiner's rejection is on pages 11 through 14 of the Answer.

The Examiner has rejected claims 5 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Chau, Nguyen, and Deshpande. The Examiner's rejection is on pages 14 through 15 of the Answer.

The Examiner has rejected claims 16 through 22, 24 through 26, and 28 under 35 U.S.C. § 103(a) as being unpatentable over Chau, Nguyen, Deshpande, and Wieczorek. The Examiner's rejection is on pages 15 through 16 of the Answer.

The Examiner has rejected claim 23 under 35 U.S.C. § 103(a) as being unpatentable over Chau, Nguyen, Deshpande, Wieczorek, and Wu. The Examiner's rejection is on page 16 of the Answer.

The Examiner has rejected claim 31 under 35 U.S.C. § 103(a) as being unpatentable over Chau, Nguyen, Deshpande, Wieczorek and Tsai. The Examiner's rejection is on page 17 of the Answer.

ISSUES

Obviousness rejections based upon Bai and Deshpande

Claims 1 through 6, 9 through 12, and 14

Appellants argue on pages 13 and 14 of the Brief[3] that the Examiner's rejection of claims 1 through 6, 9 through 12, and 14[4] under 35 U.S.C. § 103(a) is in error. Appellants states that "Bai et al. uses a layer [referring to layer 206 in figure 2a-2c] between the metal and conductive layers to avoid the silicide process from unwanted attack of the underlying conductive gate structure." Appellants argue that this differs from the claim 1 invention which states no interceding steps between the deposition of the conductive layer and the amorphous silicon (which is used to form the metal silicide structure that is directly on the gate structure).

Thus, we are presented with the issue: have Appellants shown that the Examiner erred in finding that Bai teaches the steps of forming a conductive layer and without inclusion of any intervening steps immediately forming an amorphous silicon layer and where an anneal procedure is used to form a silicide from the amorphous silicon and a metal layer formed over the amorphous silicide as recited in claim 1?

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[3] Throughout the opinion we refer to the corrected Brief dated Jan. 22, 2008.
[4] Appellants' arguments group these claims together and we select claim 1 as representative of the group.

Claims 8, 15 through 21, 23 through 28, and 31

Appellants argue on pages 14 through 16 of the Brief that the Examiner's rejections of these claims are in error. These arguments are all directed to the same issue as raised with respect to claim 1.

Obviousness rejections based upon Chau and Nguyen

Claims 1 through 4, 6, 7, and 9

Appellants argue on pages 16 and 17 of the Brief that the Examiner's rejection is in error. Appellants state that claim 1 recites that the silicide region is formed via total consumption of the amorphous silicon. Appellants argue that Chau's teaching clearly shows only partial consumption of the silicon 512. Further, Appellants argue that Nguyen describes fabrication of the gate structure but "never claiming metal silicide formation on an underlying gate structure [is] achieved via total consumption of the components, a metal layer an amorphous silicon layer."

Thus, we are presented with the issue: have Appellants shown that the Examiner erred in finding that the combination of Chau and Nguyen teach forming a silicide layer via total consumption of the amorphous silicon shape as recited in claim 1?

Claims 5, 10, 16 through 26, 28, and 31

Appellants argue on pages 17 through 19 of the Brief that the Examiner's rejections of these claims are in error. These arguments are all directed to the same issue as raised with respect to claim 1.

PRINCIPLES OF LAW

In analyzing the scope of the claim, Office personnel must rely on Appellant's disclosure to properly determine the meaning of the terms used in the claims. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir. 1995). "[I]nterpreting what is *meant* by a word *in* a claim 'is not to be confused with adding an extraneous limitation appearing in the specification, which is improper.'" (Emphasis original) *In re Cruciferous Sprout Litigation,* 301 F.3d 1343, 1348 (Fed. Cir. 2002) (citations and quotations omitted).

On the issue of obviousness, the Supreme Court has stated that "[t]he obviousness analysis cannot be confined by a formalistic conception of the words teaching, suggestion, and motivation." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007). Further, the Court stated "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR*, 127 S. Ct. at 1739. "One of the ways in which a patent's subject matter can be proved obvious is by noting that there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims." *Id.* at 1742.

FINDINGS OF FACT

Bai

1. Bai teaches a method of forming a polycide gate electrode for a MOSFET. Col. 1, ll. 23-31.

2. A silicon layer 204 is formed in an area of the gate. The silicon layer has a barrier layer formed on top of it. On top of the barrier layer 206 an amorphous silicon layer 208 is formed. Finally, a metal layer 218 is formed over the amorphous silicon layer. Col. 3, ll. 48-49, 66-67, col. 4, ll. 32-34, col. 5, ll. 33-35, fig 2b.
3. The layers are annealed to cause a reaction between the amorphous silicon layer 208 and the metal layer 218 to form a silicide layer 220. Col. 5, ll. 62-67, col. 6, ll. 19-20, fig. 2c.
4. The barrier layer can be made of a metal. Col. 4, ll. 17-18.

Chau

5. Chau teaches a MOS transistor with a silicide layer 524 formed over the gate. Abstract, col. 6, ll. 32, and fig 4g.
6. The silicide layer is created by forming a metal layer 522 over a reactive silicon layer 512 and annealing the two layers. Col. 6, ll. 18-28, figure 4f.
7. As can be seen by comparing figure 4g and 4f the formation of silicide layer 524, does not consume the entire silicon layer 512 (portions of layer 512 are still present in figure 4g which includes the silicide layer 524).

Nguyen

8. Nguyen teaches a process for forming MOSFET devices. Col. 1, 13-16.
9. Nguyen teaches that a silicide layer is formed by reacting a metal layer over silicon. Nguyen teaches that it is known that most or all of the silicon is consumed during the reaction. Col. 5, ll. 60-67.

ANALYSIS

Obviousness rejections based upon Bai and Deshpande

Claims 1 through 6, 9 through 12, and 14.

Appellants' arguments have not persuaded us that the Examiner erred in finding that Bai teaches the steps of forming a conductive layer and without inclusion of any intervening steps immediately forming an amorphous silicon layer and where an anneal procedure is used to form a silicide from the amorphous silicon and a metal layer formed over the amorphous silicide.

Representative claim 1 recites "forming a conductive layer on said gate insulator layer." The Examiner has found that Bai's barrier layer 206 meets this limitation. Ans. 4, 18 and 19. We find that the evidence supports this finding by the Examiner. Bai teaches that barrier layer 206 is formed over a layer 204 of silicon in the semiconductor gate. Fact 2. Further, Bai teaches that the layer is made of metal which a skilled artisan would recognize is conductive. Fact 4.

Claim 1 further recites that "without inclusion of any interceding steps immediately forming an amorphous silicon layer." The Examiner has found that Bai teaches that the formation of layer 208 meets this limitation. Ans. 4. We concur with the Examiner's finding and note that Bai teaches no step between the formation of layer 206 and amorphous silicon 208. Fact 2.

Claim 1 additionally recites "performing an annealing procedure ... to form a second metal silicide region directly on said conductive gate structure from an overlaying second portion of said metal layer via total consumption of said amorphous silicon shape." The Examiner has found that Bai teaches this limitation in that Bai teaches that an annealing process causes metal

layer 218 and silicon layer 208 to combine. Ans. 5. We find that the facts support this finding. Facts 3. We additionally note that Bai teaches that the silicon layer 208 is consumed by the annealing process. Col. 4, ll. 37-42.[5]

Appellants' arguments assert that Bai's teaching of using a protective layer 206 does not meet the limitation of no interceding steps between deposition of the conductive layer and the amorphous silicon. The assumption in Appellants' argument seems to be that Bai's layer 204 meets the claimed conductive layer on the gate insulating layer. However, as discussed above, the Examiner has found that the formation of Bai's layer 206 meets the conductive layer, and that the formation of Bai's layer 208 meets the claimed amorphous silicon layer. Appellants have not identified why these findings by the Examiner do not teach the claim steps of forming the conductive layer and amorphous silicon layer. Thus, Appellants have not persuaded us of error in the Examiner's rejection of claim 1 based upon the combination of Bai and Deshpande. Appellants' arguments have grouped claims 2 through 6, 9 through 12 and 14 with claim 1. Accordingly, we sustain the Examiner's rejection of claims 1 through 6, 9 through 12 and 14 as being unpatentable over Bai and Deshpande.

Claims 8, 15 through 21, 23 through 28, and 31.

As discussed above, Appellants' arguments directed to the rejections of claims 8, 15 through 21, 23 through 28, and 31 based upon the teachings

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[5] We note that this passage contains a typographical error in that it refers to the top amorphous silicon layer as item 202 and should refer to the top amorphous silicon layer 208.

of Bai and Deshpande coupled with additional references present the same issues as discussed with respect to claim 1. Accordingly, we sustain the Examiner's rejections of claims 8, 15 through 21, 23 through 28 and 31 for the reasons discussed with respect to claim 1.

Obviousness rejections based upon Chau and Nguyen

Claims 1 through 4, 6, 7, and 9

Appellants have not persuaded us that the Examiner erred in finding that the combination of Chau and Nguyen teach forming a silicide layer via total consumption of the amorphous silicon shape as recited in claim 1. As discussed above, claim 1 recites "performing an annealing procedure ... to form a second metal silicide region directly on said conductive gate structure from an overlaying second portion of said metal layer via total consumption of said amorphous silicon shape." We note that contrary to Appellants' arguments, claim 1 only requires that the silicon be totally consumed and does not require the metal to be totally consumed. The Examiner has found that Chau does not teach that the formation of the silicide layer 524 completely consumes the silicon layer. Answer 11 and 12. We concur with this finding. Fact 7. The Examiner finds that Nguyen teaches that it was known that in the creation of a silicide layer, all of the underlying silicon may be consumed. Ans. 12. Similarly, we find ample evidence to support this finding by the Examiner. Nguyen teaches, a process to create a silicide layer similar to that discussed in Chau, forming a metal over reactive silicon and reacting the two layers. Fact 9. Further, Nguyen teaches that such a process can be used to consume most or all of the silicon. Fact 9.

Appellants' argument, that Nguyen does not teach that the silicide over the gate regions is not persuasive as the assertion is not supported by the teachings of Nguyen. Nguyen discusses the silicide layer as item 85. As is clear from figure 8, there are several layers identified as layer 85, some are over the doped regions 42 and others are on the upper part of gate electrode 70. Thus, Appellants' arguments have not persuaded us of error in the Examiner's rejection of claim 1 over the combination of Chau and Nguyen. Appellants' arguments have grouped claims 2 through 4, 6, 7, and 9 with claim 1. Accordingly, we sustain the Examiner's rejection of claims 1 through 4, 6, 7, and 9 over the combination of Chau and Nguyen.

Claims 5, 10, 16 through 26, 28, and 31.

As discussed above, Appellants' arguments directed to the rejections of claims 5, 10, 16 through 26, 28, and 31 based upon the teachings of Chau and Nguyen coupled with additional references present the same issues as discussed with respect to claim 1. Accordingly, we sustain the Examiner's rejections of claims 5, 10, 16 through 26, 28, and 31 for the reasons discussed with respect to claim 1.

CONCLUSIONS

1. Under 35 U.S.C. § 103(a), Appellants have not shown that the Examiner erred in finding that Bai teaches the steps of forming a conductive layer and without inclusion of any intervening steps immediately forming an amorphous silicon layer and where an anneal procedure is used to form a silicide from the amorphous silicon and a metal layer formed over the amorphous silicide.

2. Under 35 U.S.C. § 103(a), Appellants have not shown that the Examiner erred in finding that the combination of Chau and Nguyen teach forming a silicide layer via total consumption of the amorphous silicon shape.

ORDER

The decision of the Examiner to reject claims 1 through 12, 14 through 28, and 31 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

KIS

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